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EXAMINER	
SMITH, CHENEA	

ART UNIT	PAPER NUMBER
2623	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,311	FYE, JAMES C.	
	Examiner	Art Unit	
	CHENEA P. SMITH	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to communications filed on 12/17/2007. Claims 26 and 28 are original. Claims 1-25 and 27 are amended. Claim 29 is cancelled. Claims 1-28 are pending in this action.

Response to Arguments

2. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 7-8, 11-13, 19 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (US20040003399, hereinafter Cooper).

Regarding claims 1, 7 and 19, Reitmeier discloses an apparatus for display of video data, the apparatus comprising:

a plurality of video decoders (video decoders 15A and 15B, see col 3, lines 51-57 and Fig. 1), each video decoder comprising:

an output (see Fig. 1), and

an input configured to be coupled to a video source (see Fig. 1), to receive video data from the video source, and to decode the received video data (see Fig. 1),

a switch network (switch 20, see Fig. 1) including an output (SO2 and SO1, see Fig. 1) and an input (I2 and I1, see Fig. 1) coupled to the video decoder outputs (see Fig. 1), and

a plurality of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35), each video processing pipeline including an input coupled to the switch network output (see Fig. 1), wherein the switch network is configured to connect any of the video decoder outputs to any of the video processing pipeline inputs (see col 3, lines 60-67).

Reitmeier does not specifically disclose a plurality of video sources, or video decoders coupled to different video sources.

In an analogous art, Cooper discloses a plurality of video sources (see Fig. 4), and video decoders coupled to different video sources (see Fig. 4).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include a plurality of video sources, and video

decoders coupled to different video sources, as disclosed by Cooper, for the advantage of for the allowing a viewer to view both television content and content from another source, while reducing the latency of receiving the signals.

Regarding claim 4, Reitmeier in view of Cooper discloses a plurality number of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35, see Reitmeier, Fig. 1) configured to process decoded video data of a plurality of video sources (see Cooper, Fig. 4) received from a plurality of video decoders (see Reitmeier, col 3, lines 60-67).

Regarding claim 8, Reitmeier in view of Cooper discloses a greater number of video decoders (see Cooper, claim 32) than video processing pipelines (see Reitmeier, Fig. 1).

Regarding claim 11, Reitmeier in view of Cooper discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, a frame in the video data (see Cooper, [0039], lines 1-10).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, a frame in the video data, as disclosed by Cooper, for the advantage of allowing a user to seamlessly switch channels.

Regarding claim 12, Reitmeier in view of Cooper discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, a field of a frame in the video data (see Cooper, [0039], lines 1-10).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include decoding, with a plurality of video decoders, a

portion of video data comprises decoding, with the plurality of video decoders, a frame in the video data, as disclosed by Cooper, for the advantage of allowing a user to seamlessly switch channels while keeping memory usage to a minimum to improve access time to the I frame.

Regarding claim 13, Reitmeier in view of Cooper discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders (see Cooper, [0039], lines 1-10), a scaled field of a frame in the video data (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7).

Regarding claim 26, Reitmeier in view of Cooper discloses analog video data (RF signal, see Reitmeier, Fig. 1).

5. Claims 2-3 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (previously cited), as applied to claim 1 above, and further in view of Machida (of record) and Itoh et al. (US6487719, hereinafter Itoh).

Regarding claims 2 and 20, Reitmeier in view of Cooper does not specifically disclose an image size/location logic coupled to each video processing pipeline output, the image/size location logic configured to receive a signal indicating a designated size of a display window and which of the plurality of video sources includes video data for display in the display window, the image size/location logic further configured to determine a location in the display window and a size of a part of the display window for display for the video data for each of the plurality of video sources including video for display.

In an analogous art, Machida discloses an image size/location logic (image selection means 101/adapted image synthesization means 105/screen control means 106, see Fig. 3) coupled to each video processing pipeline output (see Fig. 4), the image size/location logic configured to receive a signal indicating designated size of a display window (display window size must be designated since the sizes of the images are designated in proportion to the screen size, see col 5, lines 17-27), the image size/location logic further configured to determine a location in the display window (see col 5, lines 56-58 and col 6, line 1) and a size of a part of the display window for display for the video data for each of the and a size of a part of the display window for display for the video data for each of including video for display (see col 5, lines 17-23).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper to include an image size/location logic coupled to each video processing pipeline output, the image/size location logic configured to receive a signal indicating a designated size of a display window and which of the plurality of video sources includes video data for display in the display window, the image size/location logic further configured to determine a location in the display window and a size of a part of the display window for display for the video data for each of the plurality of video sources including video for display, as disclosed by Machida, for the advantage of providing flexibility to a system in order to effectively display multiple screens within a display.

Reitmeier in view of Cooper, and further in view of Machida does not specifically disclose an indication of which of a plurality of video sources includes video data for display in a display window.

In an analogous art, Itoh discloses an indication of which of a plurality of video sources includes video data for display in a display window (see col 12, lines 53-60).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper, and further in view of Machida to include an indication of which of a plurality of video sources includes video data for display in a display window, as disclosed by Itoh, for the advantage of conserving the processing resources of the system by only providing only the necessary processing for specific signals.

Regarding claims 3 and 21, Reitmeier in view of Cooper and Machida, and further in view of Itoh discloses a plurality of scalers (image processing means 102, see Machida, Fig. 3) coupled to a plurality of video decoders (see Cooper, Fig. 4) and a plurality of video processing pipelines (see Reitmeier, Fig. 1), wherein the plurality of scalers are each configured to scale decoded video data from the plurality of video sources (see Machida, col 5, lines 36-41 and Fig. 3) based on the determined size of the part of the display window (see Machida, col 5, lines 17-23).

6. Claims 5 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (previously cited), as applied to claim 1 above, and further in view of Machida (of record).

Regarding claims 5 and 22, Reitmeier in view of Cooper discloses a plurality of video processing pipelines (see Reitmeier, Fig. 1), and a greater number of video decoders (see Cooper, claim 32) than video processing pipelines (see Reitmeier, Fig. 1), but does not specifically

disclose a display/control logic coupled to the plurality of video processing pipelines, the display/control logic configured to control a process order of the video data from the plurality of video sources.

In an analogous art, Machida discloses a display/control logic (screen control means 106, see Fig. 3), the display/control logic configured to control a process order of the video data from the plurality of video sources (see col 5, lines 17-19).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper to include a display/control logic, the display/control logic configured to control a process order of the video data from the plurality of video sources, as disclosed by Machida, for the advantage of providing the displayed images in an order based on priority.

7. Claims 6 and 9-10, 14 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (previously cited), as applied to claims 1 and 7 above, and further in view of Miyazaki (of record).

Regarding claims 6 and 27, Reitmeier in view of Cooper discloses a plurality of video processing pipelines (see Reitmeier, Fig. 1), a plurality of video sources (see Cooper, Fig. 4) and processed decoded data (see Cooper, Fig. 4), but does not specifically discloses a memory device, or a write multiplexer coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device.

In an analogous art, Miyazaki discloses a memory device (VRAM 18A, see Fig. 1), and a write multiplexer (mux 12, see Fig. 1) coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device (see Fig. 1).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper to include a memory device, and a write multiplexer coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device, as disclosed by Miyazaki, for the advantage of sequentially storing I-frames as they are decoded, thereby reducing the latency of switching signals.

Regarding claim 9, Reitmeier in view of Cooper, and further in view of Miyazaki discloses storing a processed decoded portion of video data into a portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 10, Reitmeier in view of Cooper, and further in view of Miyazaki discloses switching the portion of the video buffer that is not updating the display with a portion of the video buffer that is updating the display, upon determining that the plurality of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35, see Reitmeier, Fig. 1) has completed processing the decoded portion of the video data (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 14, Reitmeier in view of Cooper, and further in view of Miyazaki discloses a method for displaying video data from a plurality of video sources (see Cooper, Fig. 4), comprising:

receiving the video data from the plurality of video sources (see Cooper, Fig. 4) at a first video decoder and a second video decoder (decoders 15A and 15B, see Reitmeier, Fig. 1),

decoding, via the first video decoder, a first frame of video data received from a first video source (see Reitmeier, col 3, lines 51-57 and col 5, lines 41-43),

decoding, via the second video decoder (see Reitmeier, Fig. 1), a second frame of the video data from a second video source (see Cooper, Fig. 4),

inputting the first decoded frame into a first video processing pipelines (main transport demultiplexer 35, see Reitmeier, col 4, lines 10-11) through a non-blocking switch network (see Reitmeier, col 3, lines 66-67),

inputting the second decoded frame into a second video processing pipeline (aux demux and process 30, see Reitmeier, Fig. 1) via the non-locking switch network (see Reitmeier, col 3, lines 66-67),

processing, by the first video processing pipeline, the first decoded frame (see Reitmeier, Fig. 1),

processing, by the second video processing pipeline, the second decoded frame (see Reitmeier, Fig. 1),

transmitting the processed first decoded frame into a first portion (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14) of a video buffer for updating the display with the processed first decoded frame (see Reitmeier, Fig. 1 and col 3, lines 66-67 and col 4, lines 63-65), and

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 28, Reitmeier in view of Cooper, and further in view of Miyazaki discloses a clock multiplier network (see Miyazaki, col 13, line 35), the clock multiplier network controlling a rate of operation of the write multiplexer (see col 13, lines 35-37).

8. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (previously cited) and Miyazaki (of record), as applied to claim 14 above, and further in view of Miura (of record).

Regarding claim 15, Reitmeier in view of Cooper and Miyazaki discloses processing, by a first video processing pipeline, a decoded first frame (see Reitmeier, col 3, lines 51-57 and col 5, lines 41-33), but does not specifically disclose determining whether a first video source coupled to the first video processing pipeline is in a failed state.

In an analogous art, Miura discloses determining whether a first video source coupled to the first video processing pipeline is in a failed state (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper and Miyazaki to include determining whether a first video source coupled to the first video processing pipeline is in a failed state, as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 16, Reitmeier in view of Cooper and Miyazaki, and further in view of Miura discloses processing, by a first video processing pipelines (main transport demux unit 35, see Reitmeier, Fig. 1), a first decoded frame comprising outputting a blacked out frame for a first

video source upon determining that the first video source is in a failed state (see Miura, col 20, lines 49-54).

Regarding claim 17, Reitmeier in view of Cooper and Miyazaki, and further in view of Miura discloses switching a configuration of a second portion of a video buffer that is not updating a display with a part of a video buffer that is updating the display, upon determining that the first and second video processing pipelines (aux demux processing unit 30 and main transport demux unit 35, see Reitmeier, Fig. 1) have completed processing the first and second decoded frames (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (previously cited) and Miyazaki (of record), as applied to claim 14 above, and further in view of Machida (of record).

Regarding claim 18, Reitmeier in view of Cooper and Miyazaki discloses scaling first and second decoded frames (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7), but does not specifically disclose scaling based on image size and the number of video sources.

In an analogous art, Machida discloses scaling based on image size and the number video sources (see Machida, col 5, lines 45-48).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper and Miyazaki to include scaling based on image size and the number of video sources, as disclosed by Machida, for the advantage of effectively providing multiple images to a user that efficiently fit's the user's particular display device.

10. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (of record) in view of Cooper (previously cited), as applied to claim 19 above, and further in view of Miura (of record).

Regarding claim 23, Reitmeier in view of Cooper discloses a video processing pipeline (main transport demux unit 35, see Reitmeier, Fig. 1), but does not specifically disclose executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time.

In an analogous art, Miura discloses executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Cooper to include executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time, as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 24, Reitmeier in view of Cooper, and further in view of Miura discloses a video fail operation comprising an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the plurality of video sources (see Miura, col 20, lines 49-54).

Regarding claim 25, Reitmeier in view of Cooper, and further in view of Miura discloses a video fail operation comprising an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure (see Miura, col 20, lines 49-54 and col 36, lines 20-33).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHENEA P. SMITH whose telephone number is (571)272-9524. The examiner can normally be reached on Monday through Friday, 7:30 am - 5:00 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Grant can be reached on (571) 272-7294. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chenea P. Smith/
Examiner, Art Unit 2623

/Christopher Grant/

Supervisory Patent Examiner, Art Unit 2623